

## Abstract

### Memory Device

5 A memory device includes a memory node (1) to which charge is written through a tunnel barrier configuration (2) from a control electrode (9). The stored charge effects the conductivity of a source/drain path (4) and data is read by monitoring the conductivity of the path. The charge barrier configuration comprises a multiple tunnel barrier configuration, which may comprise alternating layers (16) of polysilicon of 3nm thickness and layers (15) of  $\text{Si}_3\text{N}_4$  of 1nm thickness, overlying  
10 polycrystalline layer of silicon (1) which forms the memory node. Alternative barrier configurations (2) are described, including a Schottky barrier configuration, and conductive nanometre scale conductive islands (30, 36, 44), which act as the memory node, distributed in an electrically insulating matrix.

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